REMARKS

These remarks are responsive to the Office Action dated April 7, 2003. Claims 1-9 are pending in the present application. Claims 1-9 have been rejected. Claims 1 and 6-9 have been amended to further define the scope and novelty of the present invention, and to correct typographical and grammatical errors. New claim 10 has been added. Accordingly, claims 1-10 are pending. For the reasons set forth more fully below, Applicants respectfully submit that the claims are allowable. Consequently, reconsideration, allowance and passage to issue are respectfully requested.

35 USC §102 Rejections

Independent claims 1, 6, 8, and 9

For ease of discussion independent claims 1, 6, 8, and 9 are provided below for ease of review:

1. (currently amended) A flip-flop comprising:
a first latch for receiving at least one bit;
a second latch coupled to the first latch for storing the at least one bit from the first latch, wherein the size of the second latch is minimized to reduce power consumption; and
a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a first clock to the first latch is active and for outputting the at least one bit from the second latch when a second clock to the second latch is active.

6. (currently amended) A flip-flop comprising:
a master latch for receiving at least one bit;
a slave latch coupled to the master latch for storing the at least one bit from the master latch wherein the size of the latch is minimized to reduce power consumption; and
a multiplexor coupled to the master latch and to the slave latch for outputting the at least one bit from the master latch when a first clock to the master latch is active and for outputting the at least one bit from the slave latch when a second clock to the slave latch is active.

8. (currently amended) A method for optimizing power and performance in a flip-flop, wherein the flip-flop includes a first latch and a second latch coupled to the first latch, the method comprising the steps of:

(a) receiving at least one bit into the first latch, wherein the first latch outputs the at least one bit to the second latch and to a multiplexor when a first clock to the first latch is active;

(b) outputting the at least one bit received from the first latch from the multiplexor when the first clock is active; and

(c) outputting the at least one bit received from the second latch from the multiplexor when a second clock to the second latch is active.

9. (currently amended) A flip-flop comprising:

a master latch for receiving at least one bit;

a slave latch coupled to the master latch for storing the at least one bit, wherein the size of the second latch is minimized to reduce power consumption; and

a shunt multiplexor coupled to the master latch and to the slave latch for receiving the at least one bit, for outputting the at least one bit from the master latch when a first clock to the master latch is active, and for outputting the at least one bit from the slave latch when a second clock to the slave latch is active.

The Examiner has stated:

Claims 1-9 are rejected under 35 USC 102(e) as being anticipated by Gregor et al, or under 35 USC 102(b) as being anticipated by Ovens et al.

Note Fig. 2 of Gregor et al, where the master latch is 20, the slave latch is 22 and the MUX is 24. In Ovens et al, the master latch is 14, the slave latch is 40 and the MUX is 66 (Fig. 1). Note also Fig. 2 of Ovens et al.

Applicants respectfully traverse the Examiner's rejections.

The present invention as recited in varying scope in amended independent claims 1, 6, 8, and 9 is directed toward a system and method for optimizing power consumption in a flip-flop. The flip-flop comprises a first latch for receiving at least one bit and a second latch coupled to the first latch for storing the at least one bit from the first latch. The size of the second latch is minimized to reduce power consumption. The flip-flop also comprises a multiplexor for outputting the at least one bit from the first latch when a first clock to the first latch is active and for outputting the at least one bit from the second latch when a second clock to the second latch is active (Summary and Fig. 2B and the accompanying text).

In accordance with present invention, the first clock is used to pass data at a significantly fast rate by outputting data directly from the first latch to the multiplexor. In

addition, the second clock is used to store data in the second latch and later output the data to the multiplexor. Typically, in a slave configuration, the most performance-critical function is the launch time of slave latch (i.e., the second latch). Here, however, the first latch performs the most performance-critical function because it passes data directly to the multiplexor. The second latch no longer serves a performance-critical function because it is used to store data. Because the second latch does not serve a performance-critical function, it can be implemented using minimum sized devices to reduce power consumption (Specification generally, Summary).

Gregor discloses a scannable double-edge-triggered flip-flop having two latches and a multiplexor, all of which are driven by a single clock. Each latch has a plurality of inputs and is coupled to the clock, which provides a clock signal, via a means for providing a delayed version of the clock signal. The multiplexor has (i) inputs fed by outputs of the latches, and (ii) a select input fed by the clock signal, and means for providing a select signal for selecting the latch whose clock is inactive. Each latch has a scan input gate and a scan output gate, and the scan output of the first latch is applied to the scan input of the second latch to form a scannable latch pair (Abstract and Fig. 2).

However, Gregor does not teach or suggest a first latch with a first clock and second latch with a second and independent clock. Thus, the multiplexor of Gregor does not output at least one bit from the first (or master) latch when a first clock to the first (or master) latch is active and for outputting the at least one bit from the second (or slave) latch when a second clock to the second (or slave) latch is active, as recited in amended independent claims 1, 6, 8, and 9. In contrast, Gregor discloses **a single clock** to the first

any claims don't recite that the 2nd clock is "independent" of 1st clock

and second latches, which selects from the first latch when the clock=0 and selects from the second latch when the clock=1 (column 3, lines 14-16).

Because Gregor discloses that **a single clock** drives both of the latches and the multiplexor and that the multiplexor outputs data, **alternating continuously between both latches** as long as the clock cycles, the second latch in Gregor serves a performance-critical function. The size of the second latch cannot be minimized to reduce power consumption. Thus, Gregor does not achieve the benefits of a reduction in power consumption as with the present invention. Therefore, Gregor fails to teach or suggest the second latch wherein the size of the second latch is minimized to reduce power consumption, and the multiplexor in cooperation with the first and second clocks, in combination with the other elements recited in amended independent claims 1, 6, 8, and 9.

Ovens discloses circuitry for latching a logic state. The circuitry includes two latches coupled to the inputs of a multiplexor. The multiplexor outputs data alternating between its two inputs. The output of the second latch has an output coupled to another input of the multiplexor. The circuitry includes elements for reducing the clock-to-Q time for its output Q (Abstract, Summary, and Fig. 4).

However, like Gregor, a single clock in Ovens drives both the first and second latches and the multiplexor. The multiplexor of Ovens outputs data, **alternating continuously between the two latches** as long as the clock cycles. Referring to Fig. 4, when the clock signal is high (where its inverted signal would thus be low), the multiplexor outputs the bit at one of its inputs 64, and when the clock signal is low (where its inverted signal would be high), the multiplexor outputs the bit at its other input

68. Because Ovens discloses that a single clock drives both the first latch and the second latch to pass data through the multiplexor, the second latch in Ovens serves a performance-critical function. The size of the second latch **cannot** be minimized to reduce power consumption. Thus, Ovens does not achieve the benefits of a reduction in power consumption as with the present invention. Therefore, Ovens fails to teach or suggest the second latch wherein the size of the second latch is minimized to reduce power consumption, and the multiplexor in cooperation with the first and second clocks, in combination with the other elements recited in amended independent claims 1, 6, 8, and 9. Accordingly, these claims are allowable over the cited references.

Remaining dependent claims

Dependent claims 2-5, and 7 depend from claims 1 and 6, respectively. Accordingly, the above-articulated arguments related to claims 1 and 6 apply with equal force to claims 2-5, and 7 and are thus allowable over the cited references for at least the same reasons as claims 1 and 6.

New Claim 10

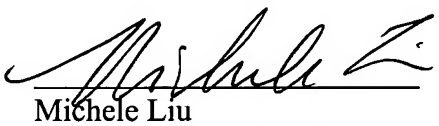
New independent claim 10 has been added to further define the scope and novelty of the present invention. Support for claim 10 is found in Fig. 2A and the accompanying text. No new matter has been presented. Applicants assert that claim 10 is allowable over the cited references for at least the same reasons stated above.

Conclusion

In view of the foregoing, Applicants submit that claims 1-10 are patentable over the cited references. Applicants, therefore, respectfully request reconsideration and allowance of the claims as now presented.

Applicants' attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,



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